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1. **Cost and performance analysis for mixed-signal system implementation: system-on-chip or package?**
Shen, M.; Li-Rong Zheng; Tenhunen, H.;
Electronics Packaging Manufacturing, IEEE Transactions on [see also Components, Packaging an Technology, Part C: Manufacturing, IEEE Transactions on]
Volume 25, Issue 4, Oct. 2002 Page(s):262 - 272
Digital Object Identifier 10.1109/TEPM.2002.807721
AbstractPlus | References | Full Text: PDF(755 KB) IEEE JNL
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2. **Preventing a "noisequake" [substrate noise analysis]**
Ponnapalli, S.; Verghese, N.; Wen Kung Chu; Coram, G.;
Circuits and Devices Magazine, IEEE
Volume 17, Issue 6, Nov. 2001 Page(s):19 - 28
Digital Object Identifier 10.1109/101.968913
AbstractPlus | References | Full Text: PDF(900 KB) IEEE JNL
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3. **A 2.6-GByte/s multipurpose chip-to-chip interface**
Lau, B.; Yiu-Fai Chan; Moncayo, A.; Ho, J.; Allen, M.; Salmon, J.; Liu, J.; Muthal, M.; Lee, C.; Nguy Leddige, M.; Kuojim Huang; Wei, J.; Leung Yu; Tarver, R.; Yuwen Hsia; Vu, R.; Tsern, F.; Haw-Jyh Nguyen, D.; Donnelly, K.; Crisp, R.;
Solid-State Circuits, IEEE Journal of
Volume 33, Issue 11, Nov. 1998 Page(s):1617 - 1626
Digital Object Identifier 10.1109/4.726545
AbstractPlus | References | Full Text: PDF(276 KB) IEEE JNL
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4. **Monolithic transformers and their application in a differential CMOS RF low-noise amplifier**
Zhou, J.J.; Allstot, D.J.;
Solid-State Circuits, IEEE Journal of
Volume 33, Issue 12, Dec. 1998 Page(s):2020 - 2027
Digital Object Identifier 10.1109/4.735543
AbstractPlus | References | Full Text: PDF(532 KB) IEEE JNL
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5. **Measurements and analyses of substrate noise waveform in mixed-signal IC environment**
Nagata, M.; Nagai, J.; Morie, T.; Iwata, A.;

Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 19, Issue 6, June 2000 Page(s):671 - 678
Digital Object Identifier 10.1109/43.848088

AbstractPlus | References | Full Text: PDF(200 KB) IEEE JNL
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6. **Modeling of substrate noise coupling for nMOS transistors in heavily doped substrates**
Shuching Hsu; Fiez, T.S.; Mayaram, K.;
Electron Devices, IEEE Transactions on
Volume 52, Issue 8, Aug. 2005 Page(s):1880 - 1886
Digital Object Identifier 10.1109/TED.2005.852171

AbstractPlus | Full Text: PDF(776 KB) IEEE JNL
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7. **Simulation and measurement of supply and substrate noise in mixed-signal ICs**
Owens, B.E.; Adluri, S.; Birrer, P.; Shreeve, R.; Arunachalam, S.K.; Mayaram, K.; Fiez, T.S.;
Solid-State Circuits, IEEE Journal of
Volume 40, Issue 2, Feb. 2005 Page(s):382 - 391
Digital Object Identifier 10.1109/JSSC.2004.841039

AbstractPlus | References | Full Text: PDF(1024 KB) IEEE JNL
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8. **Substrate coupling noise issues in silicon technology**
Jenkins, K.A.;
Silicon Monolithic Integrated Circuits in RF Systems, 2004. Digest of Papers. 2004 Topical Meetinc
8-10 Sept. 2004 Page(s):91 - 94
Digital Object Identifier 10.1109/SMIC.2004.1398175

AbstractPlus | Full Text: PDF(541 KB) IEEE CNF
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9. **IEEE Std 1100 - 2005 IEEE Recommended Practice for Powering and Grounding Electronic E**
IEEE Std 1100-2005 (Revision of IEEE Std 1100-1999)
2006 Page(s):0_1 - 589

AbstractPlus | Full Text: PDF(9973 KB) IEEE STD

10. **IEEE Std 802.3 - 2005 Part 3: Carrier sense multiple access with collision detection (CSMA/C and physical layer specifications - Section two**
IEEE Std 802.3-2005 (Revision of IEEE Std 802.3-2002 including all approved amendments)
Volume Section2, 2005 Page(s):1 - 810

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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **Methodology for I/O cell placement and checking in ASIC designs using area-array power gr**
   Buffet, P.H.; Natonio, J.; Proctor, R.A.; Sun, Yu.H.; Yasar, G.;
   Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000
   21-24 May 2000 Page(s):125 - 128
   Digital Object Identifier 10.1109/CICC.2000.852632
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Term(s): power supply w/15 noise and signal coupling and equivalent circuit*

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1 Session 5B: Embedded tutorial: CAD solutions and outstanding challenges for mixed-signal and RF IC design: CAD solutions and outstanding challenges for mixed-signal and RFIC design

Domine Leenaerts, Georges Gielen, Rob A. Rutenbar
November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Press
Full text available: pdf(1.87 MB) Additional Information: full citation, abstract, references, index terms

This tutorial paper addresses the problems and solutions that are posed by the design of mixed-signal integrated systems on chip (SoC). These include problems in mixed-signal design methodologies and flows, problems in analog design productivity, as well as open problems in analog, mixed-signal and RF design, modeling and verification tools. The tutorial explains the problems that are posed by these mixed-signal/RF SoC designs, describes the solutions and their underlying methods that exist toda ...

2 "Body coupled FingerRing": wireless wearable keyboard

Masaaki Fukumoto, Yoshinobu Tonomura
March 1997 **Proceedings of the SIGCHI conference on Human factors in computing systems**
Publisher: ACM Press
Full text available: pdf(1.06 MB) Additional Information: full citation, references, citings, index terms

Keywords: BodyNet, FingeRing, PAN, PDA, input device, interface device, keyboard, wearable computer

3 Level set and PDE methods for computer graphics

David Breen, Ron Fedkiw, Ken Museth, Stanley Osher, Guillermo Sapiro, Ross Whitaker
August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**
Publisher: ACM Press
Full text available: pdf(17.07 MB) Additional Information: full citation, abstract, citings

Level set methods, an important class of partial differential equation (PDE) methods,

define dynamic surfaces implicitly as the level set (iso-surface) of a sampled, evolving nD function. The course begins with preparatory material that introduces the concept of using partial differential equations to solve problems in computer graphics, geometric modeling and computer vision. This will include the structure and behavior of several different types of differential equations, e.g. the level set eq ...

4 Electromagnetic modeling and signal integrity simulation of power/ground networks in high speed digital packages and printed circuit boards

Frank Y. Yuan

May 1998 **Proceedings of the 35th annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(275.46 KB) Publisher Site

Additional Information: full citation, abstract, references, index terms

The electromagnetic modeling and parameter extraction of digital packages and PCB boards for system signal integrity applications are presented. A systematic approach to analyze complex power/ground structures and simulate their effects on digital systems is developed. First, an integral equation boundary element algorithm is applied to the electromagnetic modeling of the PCB structures. Then, equivalent circuits of the power/ground networks are extracted from the EM solution. In an integra ...

Keywords: custom sizing, migration, timing optimazation

5 Session 1OC: Embedded tutorial: IC power distribution challenges: Challenges in power-ground integrity

Shen Lin, Norman Chang

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design ICCAD '01**

Publisher: IEEE Press

Full text available: pdf(54.74 KB)

Additional Information: full citation, abstract, references, citings, index terms

With the advance of semiconductor manufacturing, EDA, and VLSI design technologies, circuits with increasingly higher speed are being integrated at an increasingly higher density. This trend causes correspondingly larger voltage fluctuations in the on-chip power distribution network due to IR-drop, L di/dt noise, or LC resonance. Therefore, Power-Ground integrity becomes a serious challenge in designing future high-performance circuits. In this paper, we will introduce Power-Ground integrity, ad ...

6 Unconventional human computer interfaces

Steffi Beckhaus, Ernst Kruijff

August 2004 **ACM SIGGRAPH 2004 Course Notes SIGGRAPH '04**

Publisher: ACM Press

Full text available: pdf(2.89 MB) Additional Information: full citation, abstract

This course focuses on how we can use the potential of the human body in experimental or unconventional interface techniques. It explores the biological or physiological characteristics of the separate parts of the body, from head to toe, and from skin to heart, showing how their sensor (input) and control (output) capabilities can be applied to human computer interfaces. We demonstrate a wide variety of applications that make use proven interfaces as well as extremely experimental systems. Exam ...

7 Power estimation and design tradeoffs: Implementing low-power configurable processors: practical options and tradeoffs

John Wei, Chris Rowen

June 2005 **Proceedings of the 42nd annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(694.82 KB) Additional Information: full citation, abstract, references, index terms

Configurable processors enable dramatic gains in energy efficiency, relative to traditional fixed instruction-set processors. This energy advantage comes from three improvements. First, configuration of the instruction set permits a much closer fit of the processor to the target applications, reducing the number of execution cycles required. Second, configuring the processor removes unneeded features, reducing power and area overhead. Third, automatic processor generation tools enable logic opti ...

Keywords: PVT (process, voltage, temperature), SOC (system on chip), configurable embedded processor, dynamic power, dynamic power efficiency, leakage power, low-power, scaled VDD

8 Systems 1: A wireless sensor network For structural monitoring
Ning Xu, Sumit Rangwala, Krishna Kant Chintalapudi, Deepak Ganesan, Alan Broad, Ramesh Govindan, Deborah Estrin
November 2004 **Proceedings of the 2nd international conference on Embedded networked sensor systems**
Publisher: ACM Press
Full text available: pdf(731.28 KB) Additional Information: full citation, abstract, references, index terms

Structural monitoring---the collection and analysis of structural response to ambient or forced excitation--is an important application of networked embedded sensing with significant commercial potential. The first generation of sensor networks for structural monitoring are likely to be data acquisition systems that collect data at a single node for centralized processing. In this paper, we discuss the design and evaluation of a wireless sensor network system (called Wisden for structural dat ...

Keywords: Wisden, sensor network, structural health monitoring

9 RF communication circuits: A novel high frequency, high-efficiency, differential class-E power amplifier in 0.18μm CMOS
Payam Heydari, Ying Zhang
August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**
Publisher: ACM Press
Full text available: pdf(264.23 KB) Additional Information: full citation, abstract, references, index terms

This paper presents the design of a high efficiency, low THD, 5.7GHz fully differential power amplifier for wireless communications in a standard 0.18mm CMOS technology. The power amplifier employs a fully differential class-E topology to achieve high power efficiency by exploiting its soft-switching property. In order to achieve high operating frequency, an injection-locked oscillator is utilized, which makes the output voltage of the power amplifier tuned at the input signal frequency. A compl ...

Keywords: class-E power amplifier, injection-locked, jitter, oscillator, phase noise, radio-frequency integrated circuits

10 Session 1D:issues in timing estimation: Effects of global interconnect optimizations on performance estimation of deep submicron design
Yu Cao, Chenming Hu, Xuejue Huang, Andrew B. Kahng, Sudhakar Muddu, Dirk Stroobandt, Dennis Sylvester

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Press
Full text available: pdf(116.06 KB) Additional Information: full citation, abstract, references, citings

In this paper, we quantify the impact of global interconnect optimization techniques that address such design objectives as delay, peak noise, delay uncertainty due to noise, power, and cost. In doing so, we develop a new system-performance simulation model as a set of studies within the MARCO GSRC Technology Extrapolation (GTX) system. We model a typical point-to-point global interconnect and focus on accurate assessment of both circuit and design technology with respect to such issues as induc ...

Keywords: VLSI, crosstalk noise, inductance, interconnect delay, system performance models, technology extrapolation

11 Implicit treatment of substrate and power-ground losses in return-limited inductance extraction
Dipak Sitaram, Yu Zheng, K. L. Shepard
November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**
Publisher: ACM Press
Full text available: pdf(192.35 KB) Additional Information: full citation, abstract, references, citings, index terms

Full-wave analysis, based on rigorous solution of the differential or integral form of Maxwell's equations, is too slow for all but the smallest designs. Traditional on-chip extraction engines are, therefore, being pushed to extract inductance and provide accurate high-frequency interconnect modelling while maintaining computational efficiency and capacity. This paper describes further accuracy-improving enhancements to the commecial full-chip RLCK extraction engine, Assura RLCX[1], based on the ...

12 Substrate coupling and analog synthesis: Equivalent circuit modeling of guard ring structures for evaluation of substrate crosstalk isolation
Daisuke Kosaka, Makoto Nagata
January 2006 **Proceedings of the 2006 conference on Asia South Pacific design automation ASP-DAC '06**
Publisher: ACM Press
Full text available: pdf(539.62 KB) Additional Information: full citation, abstract, references

A substrate-coupling equivalent circuit can be derived for an arbitrary guard ring test structure by way of F-matrix computation. The derived netlist represents a unified impedance network among multiple sites on a chip surface and allows circuit simulation for evaluation of isolation effects provided by guard rings. Geometry dependency of guard ring effects attributes to layout patterns of a test structure, including such as area of a guard ring as well as location distance from the circuit to ...

13 Session 37: special session: beyond low-power design: environmental energy harvesting: Circuits for energy harvesting sensor signal processing
Rajeevan Amirtharajah, Justin Wenck, Jamie Collier, Jeff Siebert, Bicky Zhou
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(3.06 MB) Additional Information: full citation, abstract, references, index terms

The recent explosion in capability of embedded and portable electronics has not been matched by battery technology. The slow growth of battery energy density has limited device lifetime and added weight and volume. Passive energy harvesting from solar

radiation, thermal sources, or mechanical vibration has potentially wide application in wearable and embedded sensors to complement batteries. The amount of energy from harvesting is typically small and highly variable, requiring circuits and archi ...

Keywords: AC power supplies, dynamic memory, energy harvesting, power-on-reset, self-timed circuits

14 High-level simulation of substrate noise generation including power supply noise coupling

Marc van Heijningen, Mustafa Badaroglu, Stéphane Donnay, Marc Engels, Ivo Bolsens

June 2000 **Proceedings of the 37th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(114.20 KB) Additional Information: full citation, abstract, references, citings, index terms

Substrate noise caused by large digital circuits will degrade the performance of analog circuits located on the same substrate. To simulate this performance degradation, the total amount of generated substrate noise must be known. Simulating substrate noise generated by large digital circuits is however not feasible with existing circuit simulators and detailed substrate models due to the long simulation times and high memory requirements. We have developed a methodology to simulate this su ...

15 Columns: Risks to the public in computers and related systems

Peter G. Neumann

January 2001 **ACM SIGSOFT Software Engineering Notes**, Volume 26 Issue 1

Publisher: ACM Press

Full text available: pdf(3.24 MB) Additional Information: full citation

16 Analysis and optimization of substrate noise coupling in single-chip RF transceiver design

Adil Koukab, Kaustav Banerjee, Michel Declercq

November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**

Publisher: ACM Press

Full text available: pdf(462.15 KB) Additional Information: full citation, abstract, references, index terms

The relentless move toward single chip integration of RF, analog and digital blocks results in significant noise coupling effects that can degrade performance and hence, should be controlled. In this paper, we propose a practical methodology that uses a suite of commercial tools in combination with a high-speed extractor based on an innovative semi-analytical method to deal with noise coupling problems, and enable RF designers to achieve a first silicon-success of their chips. The integration of ...

17 Interconnect coupling noise in CMOS VLSI circuits

Kevin T. Tang, Eby G. Friedman

April 1999 **Proceedings of the 1999 international symposium on Physical design**

Publisher: ACM Press

Full text available: pdf(742.30 KB) Additional Information: full citation, references, citings, index terms

18 Mixed-signal design and simulation: Characterizing the effects of clock jitter due to substrate noise in discrete-time D/S modulators

Payam Heydari
June 2003 **Proceedings of the 40th conference on Design automation**
Publisher: ACM Press

Full text available: pdf(415.86 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper investigates the impact of clock jitter induced by substrate noise on the performance of the oversampling DS modulators. First, a new stochastic model for substrate noise is proposed. This model is then utilized to study the clock jitter in clock generators incorporating phase-locked loops (PLLs). Next, the effect of the clock jitter on the performance of the DS modulator is studied. It will be shown that substrate noise degrades the signal-to-noise ratio of the DS modulator while the ...

Keywords: DS modulators, jitter, mixed-signal integrated circuits, phase noise, phase-locked loop, substrate noise

19 Substrate crosstalk analysis in mixed signal CMOS integrated circuits: embedded tutorial
Makoto Nagata, Atsushi Iwata
January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**
Publisher: ACM Press
Full text available: pdf(476.00 KB) Additional Information: full citation, references

20 Power Grid and Signal Integrity Analysis: Analytical signal integrity verification models for inductance-dominant multi-coupled VLSI interconnects
Seongkyun Shin, Yungseon Eo, William R. Eisenstadt, Jongin Shim
April 2002 **Proceedings of the 2002 international workshop on System-level interconnect prediction**
Publisher: ACM Press

Full text available: pdf(275.71 KB) Additional Information: full citation, abstract, references, citings, index terms

Novel signal integrity verification models for inductance-dominant RLC interconnect lines are developed by using a traveling-wave-based waveform approximation (TWA) technique. The multi-coupled line responses are decoupled into the eigenmodes of the system in order to exploit the TWA technique. Then, the response signals are mathematically represented by the linear combination of each eigenmode response based on TWA, followed by reporting the signal integrity models for the multi-coupled lines. ...

Keywords: TWA, VLSI interconnect, crosstalk, delay, glitch, ringing, signal integrity, signal integrity verification, transmission line, traveling-wave

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1 Electromagnetic modeling and signal integrity simulation of power/ground networks in high speed digital packages and printed circuit boards

Frank Y. Yuan

May 1998 **Proceedings of the 35th annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(275.46 KB) Additional Information: full citation, abstract, references, index terms

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The electromagnetic modeling and parameter extraction of digital packages and PCB boards for system signal integrity applications are presented. A systematic approach to analyze complex power/ground structures and simulate their effects on digital systems is developed. First, an integral equation boundary element algorithm is applied to the electromagnetic modeling of the PCB structures. Then, equivalent circuits of the power/ground networks are extracted from the EM solution. In an integra ...

Keywords: custom sizing, migration, timing optimazation

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Marc van Heijningen, Mustafa Badaroglu, Stéphane Donnay, Marc Engels, Ivo Bolsens

June 2000 **Proceedings of the 37th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(114.20 KB) Additional Information: full citation, abstract, references, citings, index terms

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3 Substrate coupling and analog synthesis: Equivalent circuit modeling of guard ring structures for evaluation of substrate crosstalk isolation

Daisuke Kosaka, Makoto Nagata

January 2006 **Proceedings of the 2006 conference on Asia South Pacific design automation ASP-DAC '06**

Publisher: ACM Press
Full text available: pdf(539.62 KB) Additional Information: full citation, abstract, references

A substrate-coupling equivalent circuit can be derived for an arbitrary guard ring test structure by way of F-matrix computation. The derived netlist represents a unified impedance network among multiple sites on a chip surface and allows circuit simulation for evaluation of isolation effects provided by guard rings. Geometry dependency of guard ring effects attributes to layout patterns of a test structure, including such as area of a guard ring as well as location distance from the circuit to ...

4 Session 37: special session: beyond low-power design: environmental energy harvesting: Circuits for energy harvesting sensor signal processing
Rajeevan Amirtharajah, Justin Wenck, Jamie Collier, Jeff Siebert, Bicky Zhou
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(3.06 MB) Additional Information: full citation, abstract, references, index terms

The recent explosion in capability of embedded and portable electronics has not been matched by battery technology. The slow growth of battery energy density has limited device lifetime and added weight and volume. Passive energy harvesting from solar radiation, thermal sources, or mechanical vibration has potentially wide application in wearable and embedded sensors to complement batteries. The amount of energy from harvesting is typically small and highly variable, requiring circuits and archi ...

Keywords: AC power supplies, dynamic memory, energy harvesting, power-on-reset, self-timed circuits

5 Interconnect coupling noise in CMOS VLSI circuits
Kevin T. Tang, Eby G. Friedman
April 1999 **Proceedings of the 1999 international symposium on Physical design**
Publisher: ACM Press
Full text available: pdf(742.30 KB) Additional Information: full citation, references, citings, index terms

6 Implicit treatment of substrate and power-ground losses in return-limited inductance extraction
Dipak Sitaram, Yu Zheng, K. L. Shepard
November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**
Publisher: ACM Press
Full text available: pdf(192.35 KB) Additional Information: full citation, abstract, references, citings, index terms

Full-wave analysis, based on rigorous solution of the differential or integral form of Maxwell's equations, is too slow for all but the smallest designs. Traditional on-chip extraction engines are, therefore, being pushed to extract inductance and provide accurate high-frequency interconnect modelling while maintaining computational efficiency and capacity. This paper describes further accuracy-improving enhancements to the commecial full-chip RLCK extraction engine, Assura RLCX[1], based on the ...

7 Power aware digital circuits: An energy-efficient temporal encoding circuit technique for on-chip high performance buses
Qingli Zhang, Jinxiang Wang, Yizheng Ye
April 2006 **Proceedings of the 16th ACM Great Lakes symposium on VLSI GLSVLSI '06**
Publisher: ACM Press

Full text available: pdf(343.75 KB) Additional Information: full citation, abstract, references, index terms

In this paper, we propose a novel temporal encoding circuit for generic on-chip buses that enables higher performance while reducing peak energy, average energy and peak current. The proposed circuit dynamically generates shield signals depending on the current and previous state of input data signals to eliminate the worst-case coupling-transitions between adjacent wires. Comparisons to standard on-chip buses of various lengths with optimal repeater insertion in the 0.18-?m CMOS technology show ...

Keywords: encoding, energy-efficient, on-chip buses, repeaters

8 Session 3D: Interconnect performance and reliability optimization: Coupled analysis of electromigration reliability and performance in ULSI signal nets

Kaustav Banerjee, Amit Mehrotra

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Press

Full text available: pdf(173.44 KB) Additional Information: full citation, abstract, references, index terms

In deep submicron VLSI circuits, interconnect reliability due to electromigration and thermal effects is fast becoming a serious design issue particularly for long signal lines. This paper presents for the first time a rigorous coupled analysis of AC electromigration that are prevalent in *signal lines* and thermal effects arising due to Joule heating of the wires. The analysis is applied to study the effect of technology scaling using ITRS data, wherein the effects of increasing interconne ...

9 SILCA: Fast-Yet-Accurate Time-Domain Simulation of VLSI Circuits with Strong Parasitic Coupling Effects

Zhao Li, C.-J. Richard Shi

November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society

Full text available: pdf(237.07 KB) Additional Information: full citation, abstract, index terms

We propose a new circuit analysis method, namelySemi-Implicit Linear-Centric Analysis (SILCA), for efficientSPICE-accurate transient simulation of deep-submicron VLSIcircuits with strong parasitic coupling effects introduced byinterconnect lines, common substrate, power/ground networks, etc.SILCA is based on two linear-centric techniques. First, a new semi-implicititerative numerical integration scheme is developed, whichapplies dynamic time step control accounting for stiff systems andmeanwhile ...

10 Modeling and design challenges and solutions for carbon nanotube-based interconnect in future high performance integrated circuits

Yehia Massoud, Arthur Nieuwoudt

July 2006 **ACM Journal on Emerging Technologies in Computing Systems (JETC)**, Volume 2 Issue 3

Publisher: ACM Press

Full text available: pdf(1.39 MB) Additional Information: full citation, abstract, references, index terms

Single-walled carbon nanotube (SWCNT) bundles have the potential to provide an attractive solution for the resistivity and electromigration problems faced by traditional copper interconnect as technology scales into the nanoscale regime. In this article, we evaluate the performance and reliability of nanotube bundles for both local and global interconnect in future VLSI applications. To provide a holistic evaluation of SWCNT bundles for on-chip interconnect, we have developed an efficient equiva ...

Keywords: Carbon nanotube, inductance, interconnect, nanotube bundle, resistance

11 Analysis methodologies for circuits: Predicting short circuit power from timing models

Emrah Acar, Ravishankar Arunachalam, Sani R. Nassif

January 2003 **Proceedings of the 2003 conference on Asia South Pacific design automation ASPDAC**

Publisher: ACM Press

Full text available: pdf(190.34 KB) Additional Information: full citation, abstract, references

Power dissipation is becoming a major show stopper for integrated circuit design especially in the server and pervasive computing technologies. Careful consideration of power requirements is expected to bring major changes in the way we design and analyze integrated circuit performance. This paper proposes a practical methodology to evaluate the short-circuit power of static CMOS gates via effective use of timing information from timing analysis. We introduce three methods to estimate short-circ ...

12 Fast power/ground network optimization based on equivalent circuit modeling

X.-D. Sheldon Tan, C.-J. Richard Shi

June 2001 **Proceedings of the 38th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(188.48 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents an efficient algorithm for optimizing the area of power or ground networks in integrated circuits subject to the reliability constraints. Instead of solving the original power/ground networks extracted from circuit layouts as previous methods did, the new method first builds the equivalent models for many series resistors in the original networks, then the sequence of linear programming method [9] is used to solve the simplified networks. The solutions of the original n ...

13 Substrate crosstalk analysis in mixed signal CMOS integrated circuits: embedded tutorial

Makoto Nagata, Atsushi Iwata

January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Publisher: ACM Press

Full text available: pdf(476.00 KB) Additional Information: full citation, references

14 Simulation and modeling techniques for RF/analog circuits: Efficient transient simulation for transistor-level analysis

Zhengyong Zhu, Khosro Rouz, Manjit Borah, Chung-Kuan Cheng, Ernest S. Kuh

January 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05**

Publisher: ACM Press

Full text available: pdf(139.85 KB) Additional Information: full citation, abstract, references

In this paper, we introduce an efficient transistor level simulation tool with SPICE-accuracy for deep-submicron(DSM) VLSI circuits with strong coupling effects. The new approach uses multigrid for large networks of power/ground, clock and signal interconnect. Transistor devices are integrated using a novel two-stage Newton-Raphson method to dynamically model the linear network and nonlinear devices interface. Orders of magnitude speedup over Berkeley SPICE3 is observed for sets of DSM design ci ...

15 Layout tools for analog ICs and mixed-signal SoCs: a survey

Rob A. Rutenbar, John M. Cohn

May 2000 **Proceedings of the 2000 international symposium on Physical design**
Publisher: ACM Press
Full text available: pdf(247.03 KB) Additional Information: full citation, references

16 Calculating worst-case gate delays due to dominant capacitance coupling
Florentin Dartu, Lawrence T. Pileggi
June 1997 **Proceedings of the 34th annual conference on Design automation DAC '97**
Publisher: ACM Press
Full text available: pdf(98.15 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

In this paper we develop a gate level model that allows us to determinethe best and worst case delay when there is dominant interconnectcoupling. Assuming that the gate input windows oftransition are known, the model can predict the worst and bestcase noise, as well as the worst and best case impact on delay. Thisis done in terms of a Ceff based gate model under general RCinterconnect loading conditions.

17 Analysis and optimization of substrate noise coupling in single-chip RF transceiver design
Adil Koukab, Kaustav Banerjee, Michel Declercq
November 2002 **Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design**
Publisher: ACM Press
Full text available: pdf(462.15 KB) Additional Information: full citation, abstract, references, index terms

The relentless move toward single chip integration of RF, analog and digital blocks results in significant noise coupling effects that can degrade performance and hence, should be controlled. In this paper, we propose a practical methodology that uses a suite of commercial tools in combination with a high-speed extractor based on an innovative semi-analytical method to deal with noise coupling problems, and enable RF designers to achieve a first silicon-success of their chips. The integration of ...

18 RF communication circuits: A novel high frequency, high-efficiency, differential class-E power amplifier in 0.18μm CMOS
Payam Heydari, Ying Zhang
August 2003 **Proceedings of the 2003 international symposium on Low power electronics and design**
Publisher: ACM Press
Full text available: pdf(264.23 KB) Additional Information: full citation, abstract, references, index terms

This paper presents the design of a high efficiency, low THD, 5.7GHz fully differential power amplifier for wireless communications in a standard 0.18mm CMOS technology. The power amplifier employs a fully differential class-E topology to achieve high power efficiency by exploiting its soft-switching property. In order to achieve high operating frequency, an injection-locked oscillator is utilized, which makes the output voltage of the power amplifier tuned at the input signal frequency. A compl ...

Keywords: class-E power amplifier, injection-locked, jitter, oscillator, phase noise, radio-frequency integrated circuits

19 Power Grid and Signal Integrity Analysis: Analytical signal integrity verification models for inductance-dominant multi-coupled VLSI interconnects
Seongkyun Shin, Yungseon Eo, William R. Eisenstadt, Jongin Shim

April 2002 **Proceedings of the 2002 international workshop on System-level interconnect prediction**
Publisher: ACM Press
Full text available: pdf(275.71 KB) Additional Information: full citation, abstract, references, citings, index terms

Novel signal integrity verification models for inductance-dominant RLC interconnect lines are developed by using a traveling-wave-based waveform approximation (TWA) technique. The multi-coupled line responses are decoupled into the eigenmodes of the system in order to exploit the TWA technique. Then, the response signals are mathematically represented by the linear combination of each eigenmode response based on TWA, followed by reporting the signal integrity models for the multi-coupled lines. ...

Keywords: TWA, VLSI interconnect, crosstalk, delay, glitch, ringing, signal integrity, signal integrity verification, transmission line, traveling-wave

20 Session 56: beyond-the-die circuit and system integration: System level signal and power integrity analysis methodology for system-in-package applications
Rohan Mandrekar, Krishna Bharath, Krishna Srinivasan, Ege Engin, Madhavan Swaminathan
July 2006 **Proceedings of the 43rd annual conference on Design automation DAC '06**
Publisher: ACM Press
Full text available: pdf(773.55 KB) Additional Information: full citation, abstract, references, index terms

This paper describes a methodology for performing system level signal and power integrity analyses of SiP-based systems. The paper briefly outlines some new modeling and simulation techniques that have been developed to enable the proposed methodology. Some results based on the application of this methodology on test systems are also presented.

Keywords: causality, finite difference method, modal decomposition, nodal admittance matrix method, power integrity, signal integrity, system-in-package (SiP)

WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Sunday, November 12, 2006

Hide?	Set Name	Query	Hit Count
	DB=PGPB,USPT; THES=ASSIGNEE; PLUR=YES; OP=ADJ		
☐	L4	(power supply with noise) and signal coupling and equivalent circuit? and (cell? with adjacent)	1
☐	L3	(power supply with noise) and signal coupling and (equivalent with circuit?)	13
☐	L2	breiland.in. and (power supply with noise) and signal coupling and (equivalent with circuit?)	1
☐	L1	breiland.in. and (power supply with noise) and signal coupling and equivalent with circuit?0	0

END OF SEARCH HISTORY

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First Hit | Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: US 20060047490 A1

L2: Entry 1 of 1 File: PGPB Mar 2, 2006

PGPUB-DOCUMENT-NUMBER: 20060047490
PGPUB-FILING-TYPE:
DOCUMENT-IDENTIFIER: US 20060047490 A1

TITLE: HIERARCHICAL METHOD OF POWER SUPPLY NOISE AND SIGNAL INTEGRITY ANALYSIS

PUBLICATION-DATE: March 2, 2006

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Breiland; Erik	Colchester	VT	US
Budell; Timothy W.	Milton	VT	US
Chiu; Charles S.	Essex Junction	VT	US
Clouser; Paul L.	Williston	VT	US
Erdelyi; Charles K.	Essex Junction	VT	US
Welch; Brian P.	Scotia	NY	US

US-CL-CURRENT: 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
BREILAND	19
BREILANDS	0
POWER	1658890
POWERS	104374
SUPPLY	1227827
SUPPLIES	459229
SUPPLYS	346
NOISE	491865
NOISES	46153

Hit List

First Hit | Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 13 of 13 returned.

1. Document ID: US 20060158268 A1

L3: Entry 1 of 13 File: PGPB Jul 20, 2006

PGPUB-DOCUMENT-NUMBER: 20060158268
PGPUB-FILING-TYPE:
DOCUMENT-IDENTIFIER: US 20060158268 A1

TITLE: Discrete clock generator and timing/frequency reference

PUBLICATION-DATE: July 20, 2006

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
McCorquodale; Michael Shannon	Detroit	MI	US
Pernia; Scott Michael	Pinckney	MI	US
Kubba; Sundus	Saline	MI	US
O'Day; Justin	Detroit	MI	US
Carichner; Gordon	Saline	MI	US

US-CL-CURRENT: 331/34

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

2. Document ID: US 20060158267 A1

L3: Entry 2 of 13 File: PGPB Jul 20, 2006

PGPUB-DOCUMENT-NUMBER: 20060158267
PGPUB-FILING-TYPE:
DOCUMENT-IDENTIFIER: US 20060158267 A1

TITLE: Inductor and capacitor-based clock generator and timing/frequency reference

PUBLICATION-DATE: July 20, 2006

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
McCorquodale; Michael Shannon	Detroit	MI	US
Pernia; Scott Michael	Pinckney	MI	US
Kubba; Sundus	Saline	MI	US

US-CL-CURRENT: 331/34

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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3. Document ID: US 20060152293 A1

L3: Entry 3 of 13 File: PGPB Jul 13, 2006

PGPUB-DOCUMENT-NUMBER: 20060152293
PGPUB-FILING-TYPE:
DOCUMENT-IDENTIFIER: US 20060152293 A1

TITLE: Integrated clock generator and timing/frequency reference

PUBLICATION-DATE: July 13, 2006

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
McCorquodale; Michael Shannon	Detroit	MI	US
Pernia; Scott Michael	Pinckney	MI	US
Kubba; Sundus	Saline	MI	US
O'Day; Justin	Detroit	MI	US
Carichner; Gordon	Saline	MI	US

US-CL-CURRENT: 331/74

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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4. Document ID: US 20060071734 A1

L3: Entry 4 of 13 File: PGPB Apr 6, 2006

PGPUB-DOCUMENT-NUMBER: 20060071734
PGPUB-FILING-TYPE:
DOCUMENT-IDENTIFIER: US 20060071734 A1

TITLE: Frequency controller for a monolithic clock generator and timing/frequency reference

PUBLICATION-DATE: April 6, 2006

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
McCorquodale; Michael Shannon	Detroit	MI	US
Pernia; Scott Michael	Pinckney	MI	US
Kubba; Sundus	Saline	MI	US

US-CL-CURRENT: 331/176

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

5. Document ID: US 20060071718 A1

L3: Entry 5 of 13 File: PGPB Apr 6, 2006

PGPUB-DOCUMENT-NUMBER: 20060071718
PGPUB-FILING-TYPE:
DOCUMENT-IDENTIFIER: US 20060071718 A1

TITLE: Frequency calibration for a monolithic clock generator and timing/frequency reference

PUBLICATION-DATE: April 6, 2006

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
McCorquodale; Michael Shannon	Detroit	MI	US
Pernia; Scott Michael	Pinckney	MI	US
Kubba; Sundus	Saline	MI	US
Basu; Amar Sarbbasesh	Troy	MI	US

US-CL-CURRENT: 331/16

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

6. Document ID: US 20060047490 A1

L3: Entry 6 of 13 File: PGPB Mar 2, 2006

PGPUB-DOCUMENT-NUMBER: 20060047490
PGPUB-FILING-TYPE:
DOCUMENT-IDENTIFIER: US 20060047490 A1

TITLE: HIERARCHICAL METHOD OF POWER SUPPLY NOISE AND SIGNAL INTEGRITY ANALYSIS

PUBLICATION-DATE: March 2, 2006

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Breiland; Erik	Colchester	VT	US
Budell; Timothy W.	Milton	VT	US
Chiu; Charles S.	Essex Junction	VT	US
Clouser; Paul L.	Williston	VT	US
Erdelyi; Charles K.	Essex Junction	VT	US
Welch; Brian P.	Scotia	NY	US

US-CL-CURRENT: 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 7. Document ID: US 20060017519 A1

L3: Entry 7 of 13 File: PGPB Jan 26, 2006

PGPUB-DOCUMENT-NUMBER: 20060017519
PGPUB-FILING-TYPE:
DOCUMENT-IDENTIFIER: US 20060017519 A1

TITLE: Low-latency start-up for a monolithic clock generator and timing/frequency reference

PUBLICATION-DATE: January 26, 2006

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Pernia; Scott Michael	Pinckney	MI	US
McCorquodale; Michael Shannon	Detroit	MI	US
Kubba; Sundus	Saline	MI	US

US-CL-CURRENT: 331/185

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 8. Document ID: US 6031406 A

L3: Entry 8 of 13 File: USPT Feb 29, 2000

US-PAT-NO: 6031406
DOCUMENT-IDENTIFIER: US 6031406 A
** See image for Certificate of Correction **

TITLE: Single rail regulator

DATE-ISSUED: February 29, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Drost; Robert J.	Palo Alto	CA		
Bosnyak; Robert J.	San Jose	CA		
Cruz; Jose M.	Menlo Park	CA		

US-CL-CURRENT: 327/319; 257/503, 257/523, 327/311, 327/551, 327/552, 327/565

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 9. Document ID: US 5770972 A

L3: Entry 9 of 13 File: USPT Jun 23, 1998

US-PAT-NO: 5770972

DOCUMENT-IDENTIFIER: US 5770972 A

TITLE: Coupling circuit

DATE-ISSUED: June 23, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Freuler; George H.	Moreno Valley	CA		
Collier, deceased; Edward J.	late of Anaheim	CA		
Mazi; David	Morano Valley	CA		
Middlebrook; R. David	San Dimas	CA		

US-CL-CURRENT: 330/149; 330/255

☐ 10. Document ID: US 5604463 A

L3: Entry 10 of 13 File: USPT Feb 18, 1997

US-PAT-NO: 5604463
DOCUMENT-IDENTIFIER: US 5604463 A

TITLE: Coupling circuit

DATE-ISSUED: February 18, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Freuler; George H.	Moreno Valley	CA		
Collier, deceased; Edward J.	late of Anaheim	CA		
Mazi; David	Moreno Valley	CA		
Middlebrook; R. David	San Dimas	CA		

US-CL-CURRENT: 330/149; 330/297

☐ 11. Document ID: US 5508604 A

L3: Entry 11 of 13 File: USPT Apr 16, 1996

US-PAT-NO: 5508604
DOCUMENT-IDENTIFIER: US 5508604 A

TITLE: Low voltage regulator with summing circuit

DATE-ISSUED: April 16, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Keeth; Brent	Boise	ID		

US-CL-CURRENT: 323/314; 323/316, 327/538, 327/540, 365/189.09

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | [illegible] | Claims | KWIC | Draw De

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☐ 12. Document ID: US 5384739 A

L3: Entry 12 of 13 File: USPT Jan 24, 1995

US-PAT-NO: 5384739
DOCUMENT-IDENTIFIER: US 5384739 A

TITLE: Summing circuit with biased inputs and an unbiased output

DATE-ISSUED: January 24, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Keeth; Brent	Boise	ID		

US-CL-CURRENT: 365/189.09; 323/313, 323/314, 327/361, 327/530, 327/540

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | [illegible] | Claims | KWIC | Draw De

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☐ 13. Document ID: US 4374435 A

L3: Entry 13 of 13 File: USPT Feb 15, 1983

US-PAT-NO: 4374435
DOCUMENT-IDENTIFIER: US 4374435 A

TITLE: Passenger entertainment system transducer failure detector

DATE-ISSUED: February 15, 1983

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lach; Richard F.	Hartford	CT		
Calcasola; Richard W.	Longmeadow	MA		

US-CL-CURRENT: 370/241; 381/58, 381/77

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | [illegible] | Claims | KWIC | Draw De

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Search Results - Record(s) 1 through 1 of 1 returned.

1. Document ID: US 20060047490 A1

L4: Entry 1 of 1 File: PGPB Mar 2, 2006

PGPUB-DOCUMENT-NUMBER: 20060047490
PGPUB-FILING-TYPE:
DOCUMENT-IDENTIFIER: US 20060047490 A1

TITLE: HIERARCHICAL METHOD OF POWER SUPPLY NOISE AND SIGNAL INTEGRITY ANALYSIS

PUBLICATION-DATE: March 2, 2006

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Breiland; Erik	Colchester	VT	US
Budell; Timothy W.	Milton	VT	US
Chiu; Charles S.	Essex Junction	VT	US
Clouser; Paul L.	Williston	VT	US
Erdelyi; Charles K.	Essex Junction	VT	US
Welch; Brian P.	Scotia	NY	US

US-CL-CURRENT: 703/14

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
POWER	1658890
POWERS	104374
SUPPLY	1227827
SUPPLIES	459229
SUPPLYS	346
NOISE	491865
NOISES	46153
NOIZE	81
NOIZES	2